16-BIT Single Cycle MIPS Processor

For using the MIPS PROCESSOR, run the application run.circ which is present in the directory.

| D run | 10/23/2017 6:38 PM | CIRC File | 89 KB |
|-------|--------------------|-----------|-------|
| | | | |

Once you open the file it will look something like the following.



FUNCTIONS SUPPORTED:

The processor supports the following operations:

| • | ADD | OP-000 | FUN-0000 | R-TYPE INSTRUCTION |
|---|------|--------|-----------------|---------------------------|
| • | SUB | OP-000 | FUN-0001 | R-TYPE INSTRUCTION |
| • | AND | OP-000 | FUN-0010 | R-TYPE INSTRUCTION |
| • | OR | OP-000 | FUN-0011 | R-TYPE INSTRUCTION |
| • | SLT | OP-000 | FUN-0100 | R-TYPE INSTRUCTION |
| • | JR | OP-000 | FUN-1000 | R-TYPE INSTRUCTION |
| • | LW | OP-100 | I-TYPE INSTRUCT | ΓΙΟΝ |
| • | SW | OP-101 | I-TYPE INSTRUCT | ΓΙΟΝ |
| • | BEQ | OP-110 | I-TYPE INSTRUCT | ΓΙΟΝ |
| • | ADDI | OP-111 | I-TYPE INSTRUCT | ΓΙΟΝ |
| • | SLTI | OP-001 | I-TYPE INSTRUCT | ΓΙΟΝ |
| • | J | OP-010 | J-TYPE INSTRUC | TION |
| • | JAL | OP-011 | J-TYPE INSTRUC | TION |

NOTE:

***** R-Type instruction:

3 bit opcode + 3 bit reg(S) + 3 bit reg(T) + 3 bit reg(D) + 4 bit fun

✤ I-Type instruction:

3 bit opcode + 3 bit reg(S) + 3 bit reg(T) + 7 bit Immediate value

♦ J-Type instruction:

3 bit opcode + 13 bit address

- ✤ \$0 is hardwired to 0.
- For beq instruction the offset + 4 will be the next address

EXAMPLES:

- 1. Addi \$1, \$0, 0x10 will be e08a (1110 0000 1000 1010) in machine code.
- 2. Sub \$1,\$1,\$1 (Must result in 0) will be 0491 (0000 0100 1001 0001).
- 3. J 0x20 (Must jump to 32^{nd} (0x20 th) location) will be 4020

(0100 0000 0010 0000).

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